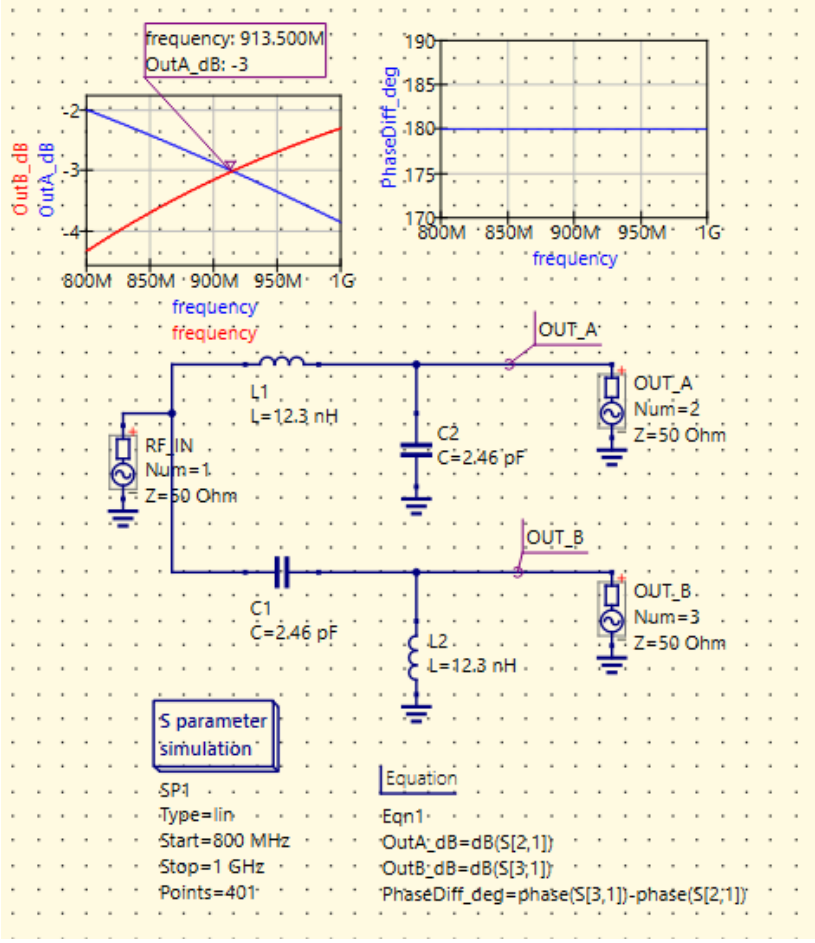
FULL BOARD SCOPE:
Antenna input
-> SMA connector for external antenna
-> Band pass filter
-> LNA and matching
-> Output conditioning (gain, attenuation, and termination for ADC) -
> Balun (Convert single-ended RF signal into a differential to reduce noise)
-> External ADC interface
For the ADC, use AD9690-1000
Power circuitry will be consistent for clean power, biasing, filtering, and decoupling

Frequency Range: 902-928 MHz
Nominal Impedance: 50 Ohms
Connector: Standard SMA male
Height: 198 mm
Mounting: Hinged Connector

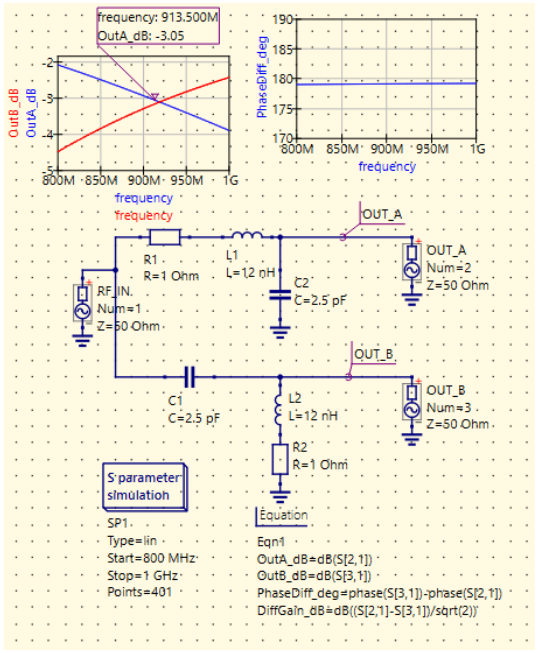
Balun Model:
Ideal Balun Simulation:

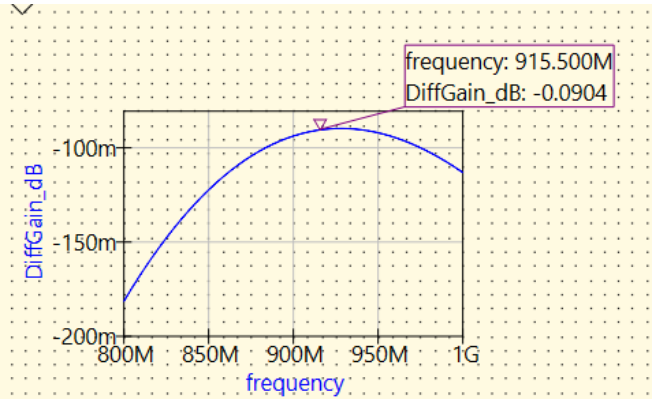


Nonideal simulation:

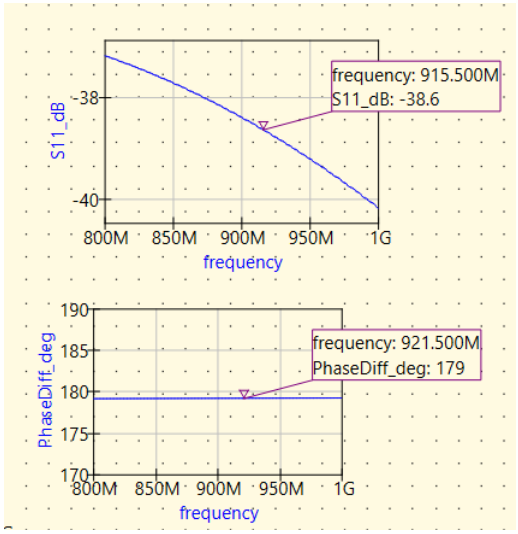
https://www.coilcraft.com/en-us/models/spice/

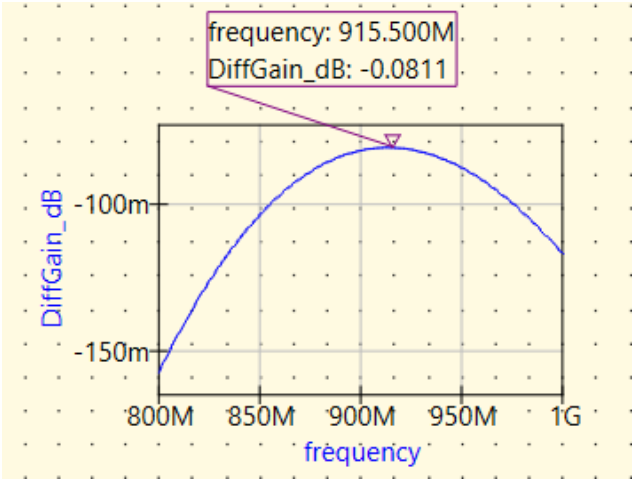
Coilcraft 0402DC-12N has a typical Q of 69 at 900MHz, using Rs = 2πfL / Q gives an impedance of approximately 1 ohm





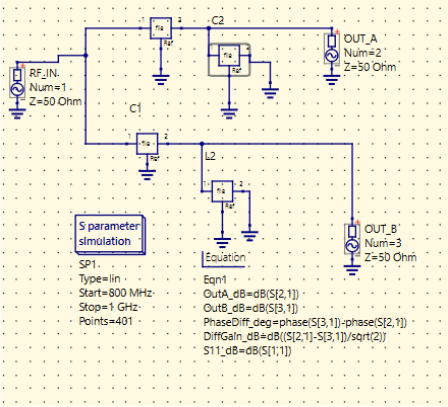
Using actual coilcraft model:

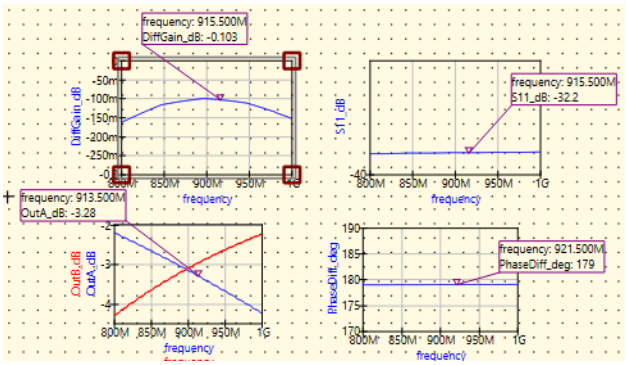


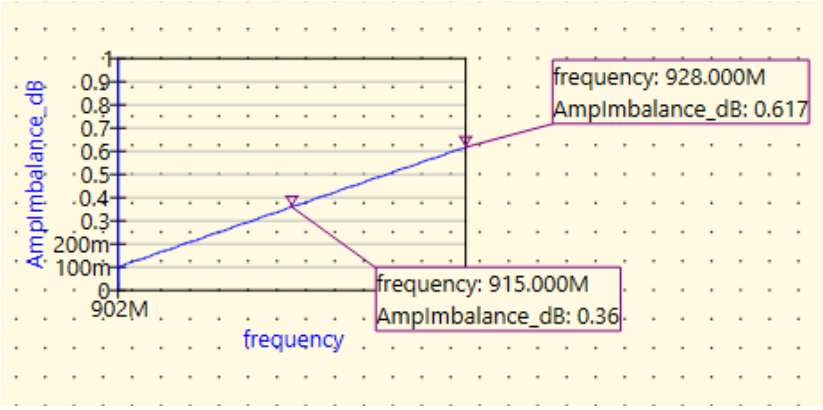


Using Nonideal Capacitor Models:
https://ds.murata.com/simsurfing/mlcc.html?lcid=en-us
GJM1555C1H2R5WB01
We can replace C1 with a series capacitor and C2 with a shunt capacitor (a shunt capacitor is the same as the one number port being connected to ground)

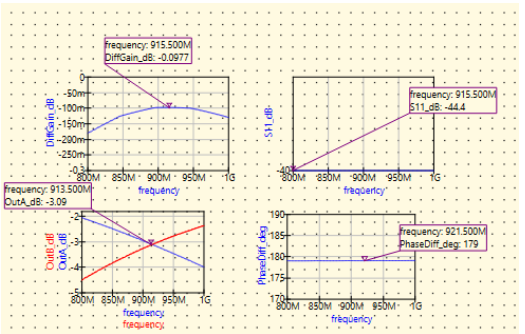
The target is less than 0.5dB amplitude imbalance across 902-928 MHz

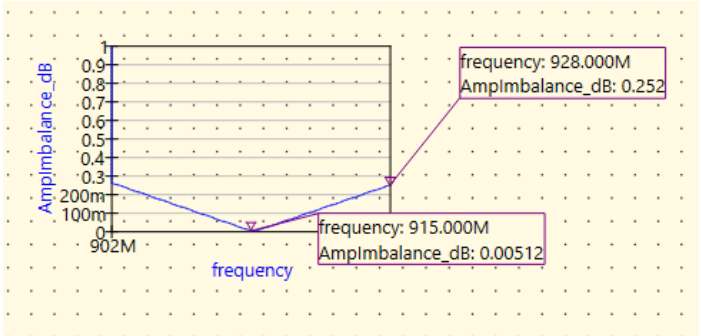






Amplitude imbalance is how close out a and out b match in magnitude, its just abs(OutA - OutB)
Initially with these capacitor models and designs, the amplitude imbalance is too high, so I am reducing the capacitor values form 2.5 pF to 2.4 pF



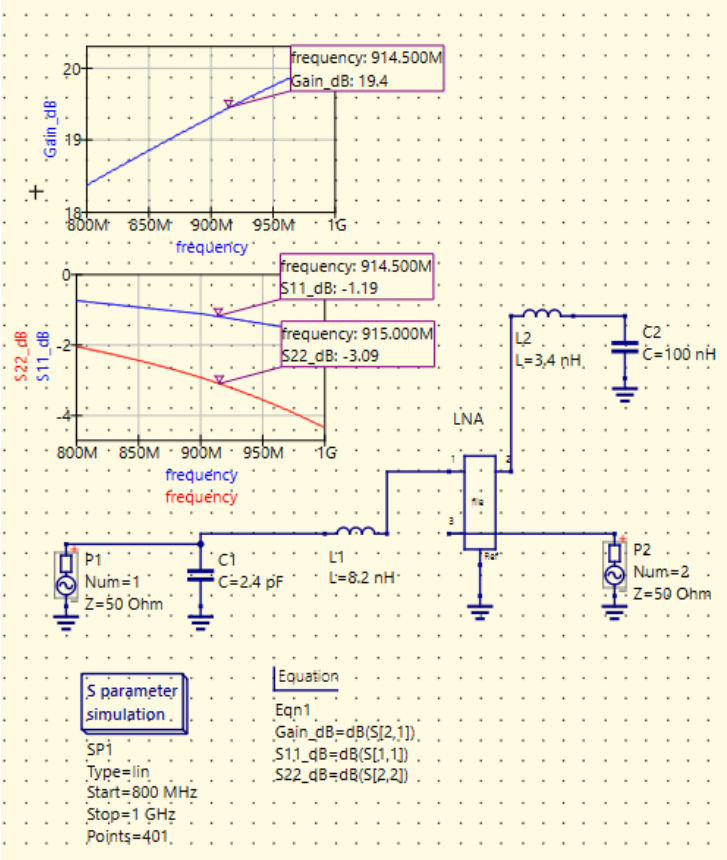


After lowering the capacitance value, these are the values we get, which are much more within our targeted operation range.
This model balun circuit will be the target one to use in my RF receiver front end PCB \

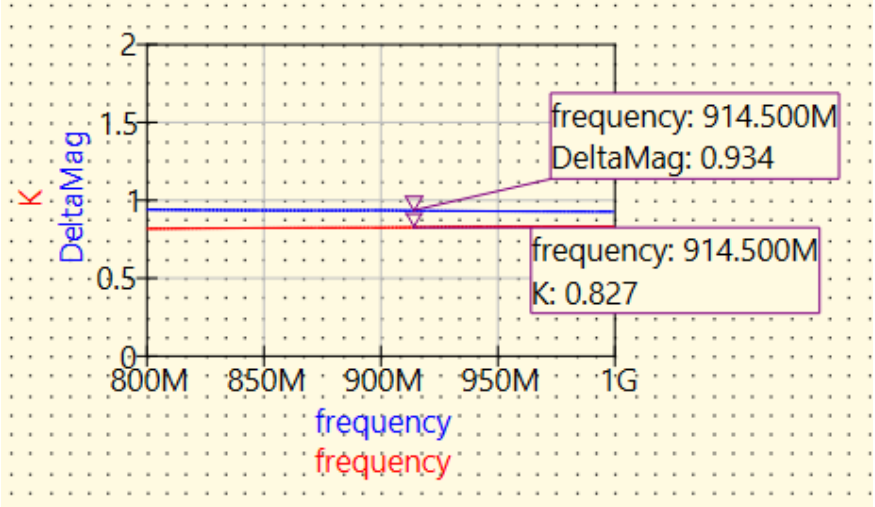
LNA MODEL:

Using the ADL5523 Low Noise Amplifier: https://www.analog.com/en/products/adl5523.html

Ideal Components (Port 1 is RF input, Port 2 is supply, Port 3 is output):



For that initial simulation, the gain looked good, but the S11 and S22 values showed that the input and output impedances were not great matches, so I wanted to check the stability of the circuit through the Rollet stability constant



K is less than 1 and DeltaMag is barely less than 1 here, meaning the system is only conditionally stable and depends on the connected impedances.

We can fix this by adding resistors at certain points to add damping that can feed RF energy back into the amplifier. They dissipate some energy and change the impedances seen by the LNA.

I tested different values for both R1 and R2 for supply and output resistors.

R1:

Resistance (Ohms)	K at 915 MHz	Gain at 915 MHz
100	0.98	18.54
68	1.057	18.12
47	1.160	17.56

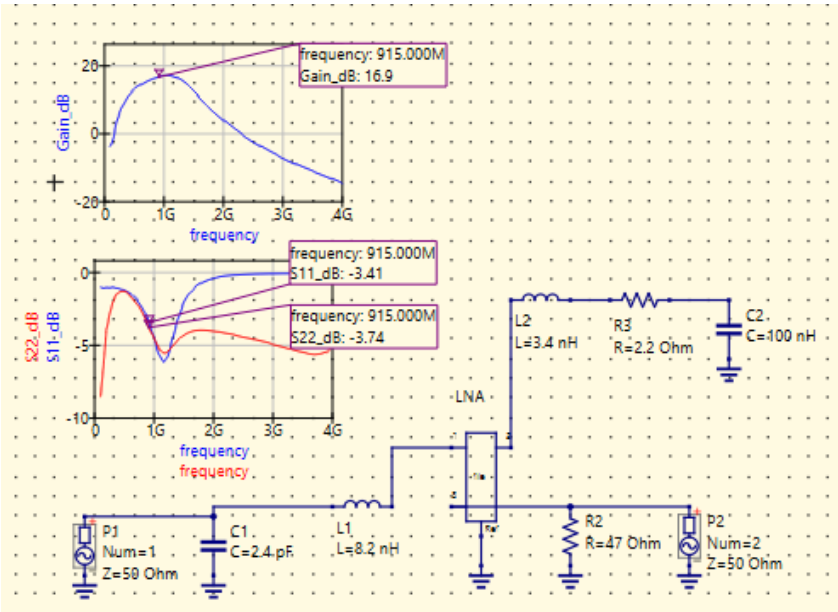
R2:

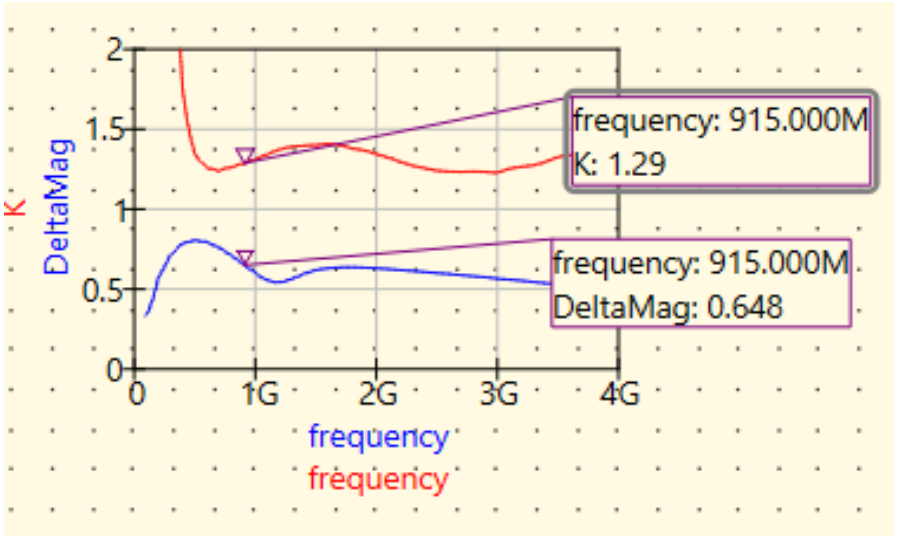
1	1.080	17.24
2.2	1.227	16.91
3.3	1.232	16.64

I chose the bolded values because they gave the most stability

By adding R2, that resistor is now in series with the output port 2 and the combined load is around 24.2 Ohms.
By Adding R1 in series with the inductor and the capacitor, it adds 2.2 Ohms of real impedance to the supply input.

After Adding the two resistors, some gain was traded for increased stability:



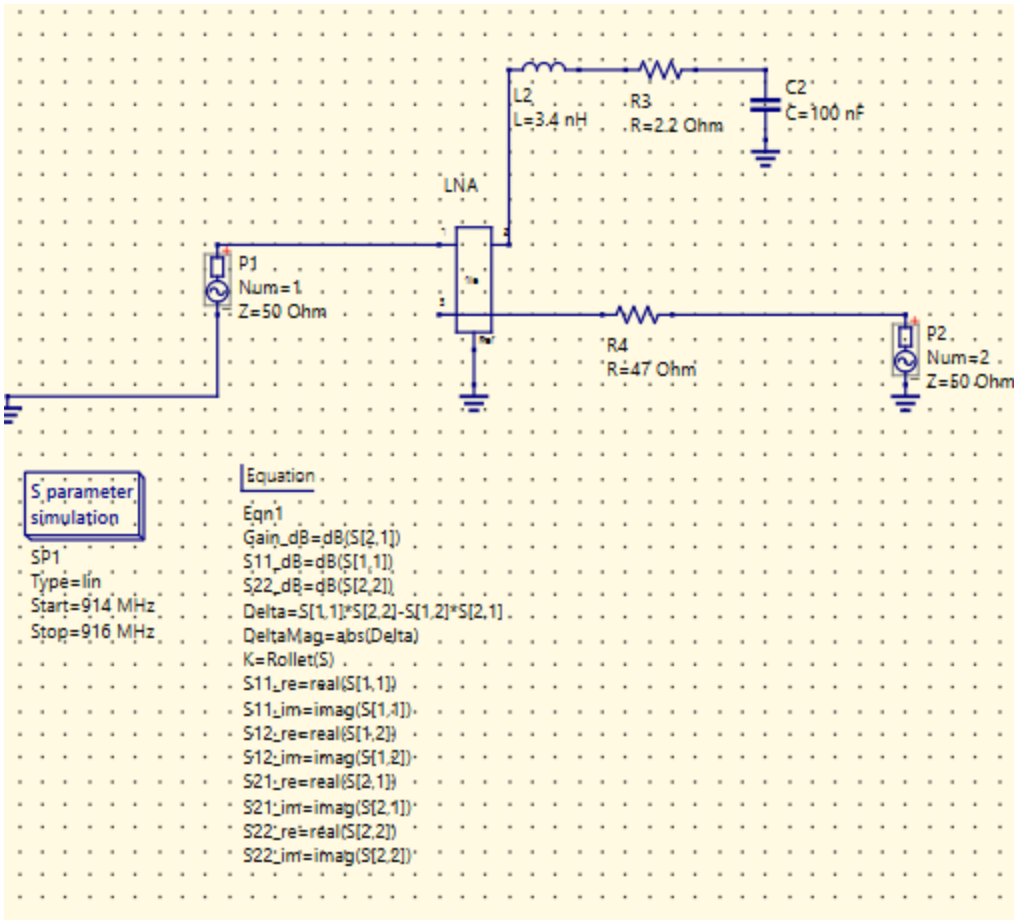


Now that we know the system is stable, we can try and match the input and output impedances for the best RF power delivery and gain
We are designing the match at:

f = 915 MHz = 915e6 Hz
Z0 = 50 ohms
Convert frequency into angular frequency:
w = 2 * pi * f
w = 5.7491e9 radians/second
We use w when calculating capacitor and inductor impedances.

First we have to get the S-parameters of teh LNA block
The block contains the manufacturer's LNA model, the 47-ohm output resistor, and the bias branch containing 3.4 nH, 2.2 ohms, and 100 nF.
I connected the 50-ohm test ports directly to the RF input and output of this block. The input and output matching networks are excluded.

Run the S-parameter simulation and find the complex values at 915 MHz.



frequency	S11_im	S11_re	S12_im	S12_re	S21_im	S21_re	S22_im	S22_re
9.14e8	-0.812	-0.0196	0.0235	0.0028	1.41	-5.37	0.207	-0.674
9.15e8	-0.811	-0.0208	0.0235	0.00282	1.42	-5.36	0.207	-0.673
9.16e8	-0.811	-0.0221	0.0236	0.00285	1.43	-5.36	0.207	-0.673

S11 = -0.02084 - j0.81130
S12 = 0.002824 + j0.023531
S21 = -5.36466 + j1.42180
S22 = -0.67338 + j0.20685
We then calculate some intermediate values to calculate the matched source and load impedance values using:

Bs = 1 + abs(S[1,1])^2 - abs(S[2,2])^2 - abs(Delta)^2
As = S[1,1] - Delta * conj(S[2,2])
Bl = 1 + abs(S[2,2])^2 - abs(S[1,1])^2 - abs(Delta)^2
Al = S[2,2] - Delta * conj(S[1,1])

The table shows the complex values in phase/magnitude so we have to convert those ourselves

frequency	Al	As	Bl	Bs
9.14e8	0.134 / 165°	0.316 / -90.5°	0.343	0.667
9.15e8	0.134 / 165°	0.316 / -90.6°	0.343	0.668
9.16e8	0.134 / 165°	0.317 / -90.6°	0.344	0.669

Bs = 0.668112
Bl = 0.343273

As = 0.316371 / -90.552 degrees
Al = 0.134002 / 165.426 degrees
Which equals
As = -0.003048 - j0.316356
Al = -0.129690 + j0.033719

Using these values we can calculate the reflection coefficients and use those to find the target impedances for the source and load we should match

Gamma_S = (Bs - sqrt(Bs^2 - 4 * abs(As)^2)) / (2 * As)
Gamma_L = (Bl - sqrt(Bl^2 - 4 * abs(Al)^2)) / (2 * Al)
Zsource = 50 * (1 + Gamma_S) / (1 - Gamma_S)
Zload = 50 * (1 + Gamma_L) / (1 - Gamma_L)

Running the simulation again gives

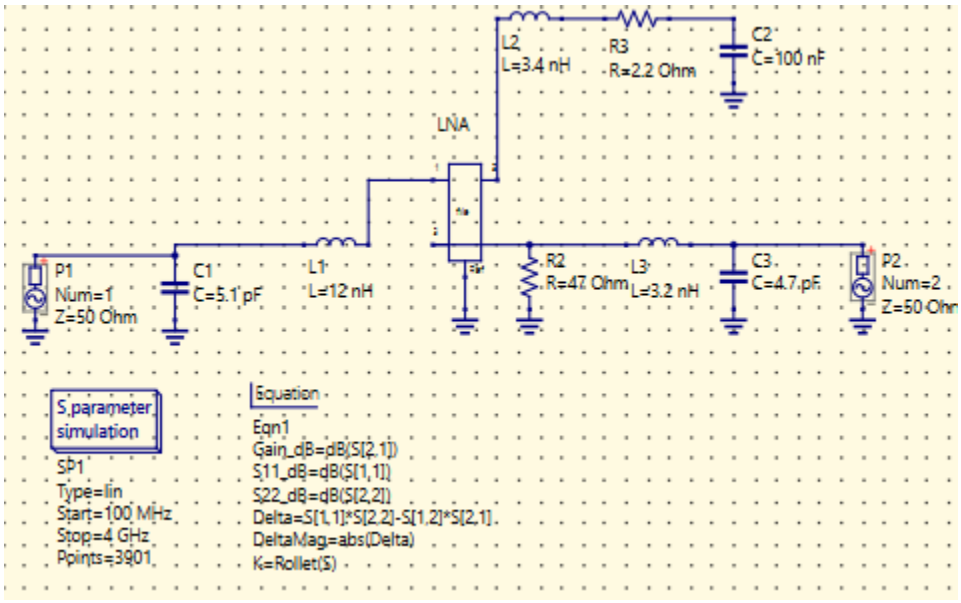
frequency	Zsource	Zload
9.14e8	49.6 / 71.3°	18.6 / -17.5°
9.15e8	49.5 / 71.3°	18.7 / -17.5°
9.16e8	49.5 / 71.3°	18.7 / -17.4°

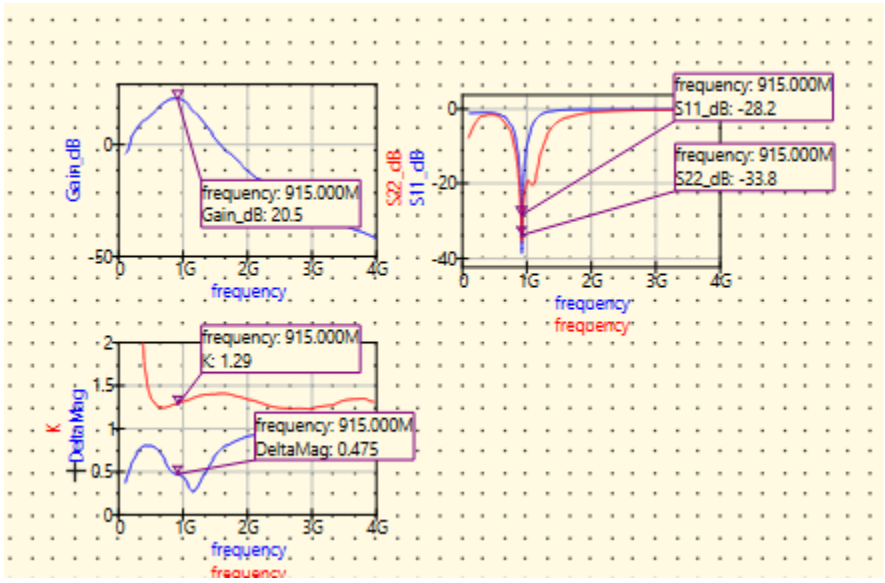
Once again , they have to be converted which then equals
Zsource = 15.91 + j46.92 ohms
Zload = 17.80 - j5.60 ohms

Now that we have the targets we can match the input and output impedances
xs = sqrt(50 / real(Zsource) - 1)
xl = sqrt(50 / real(Zload) - 1)
C1_pF = xs / (50 * wm) * 1e12
L1_nH = (imag(Zsource) + real(Zsource) * xs) / wm * 1e9
C3_pF = xl / (50 * wm) * 1e12
L3_nH = (imag(Zload) + real(Zload) * xl) / wm * 1e9
The capacitors transform the 50-ohm terminations to the required resistance and introduce capacitive reactance. The inductor adds inductive reactance to reach the targets

frequency	xl	xs	C1_pF	C3_pF	L1_nH	L3_nH
9.14e8	1.35	1.46	5.1	4.69	12.2	3.19
9.15e8	1.35	1.46	5.09	4.68	12.2	3.19
9.16e8	1.34	1.46	5.09	4.67	12.2	3.19

And so we get the values of about 5.1 pF, 4.7 pF, 12 nH, and 3.2nH



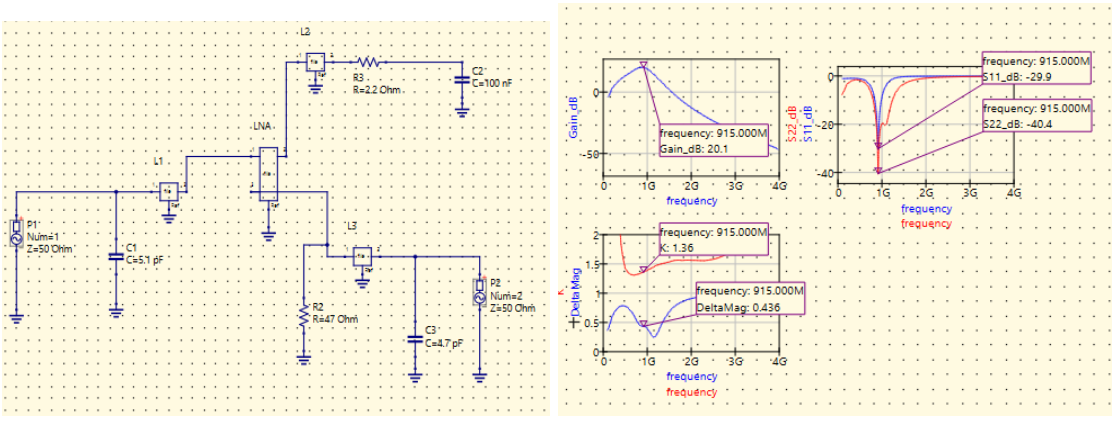


After matching impedances the power delivered is much better

After verifying the performance of the circuit with ideal components, we can move onto simulating the circuit with actual vendor components.

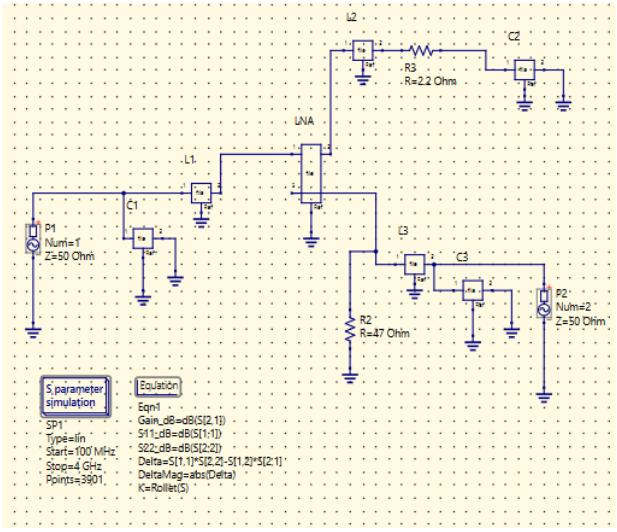
Non ideal (vendor) component simulation:

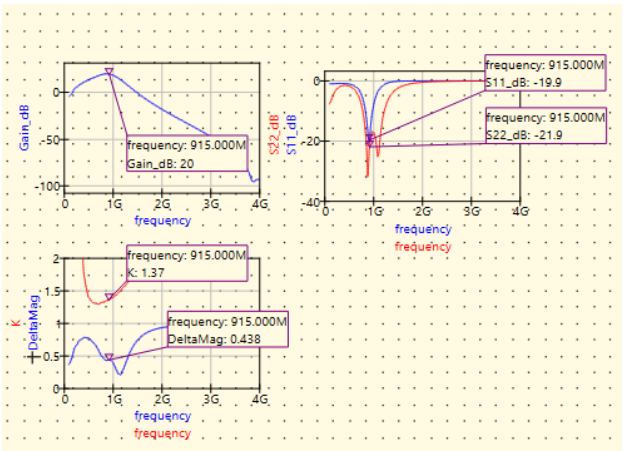
Replace inductors first using coilcraft models

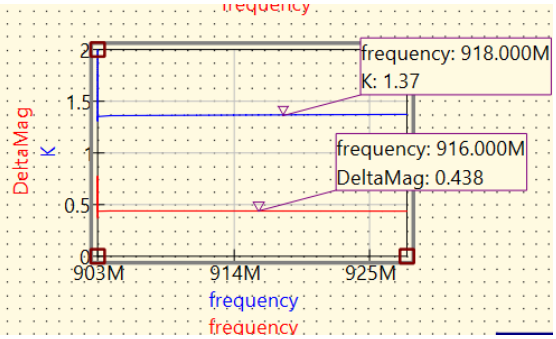


The simulated output values still are well within desired ranges

Next replace capacitors using murata models



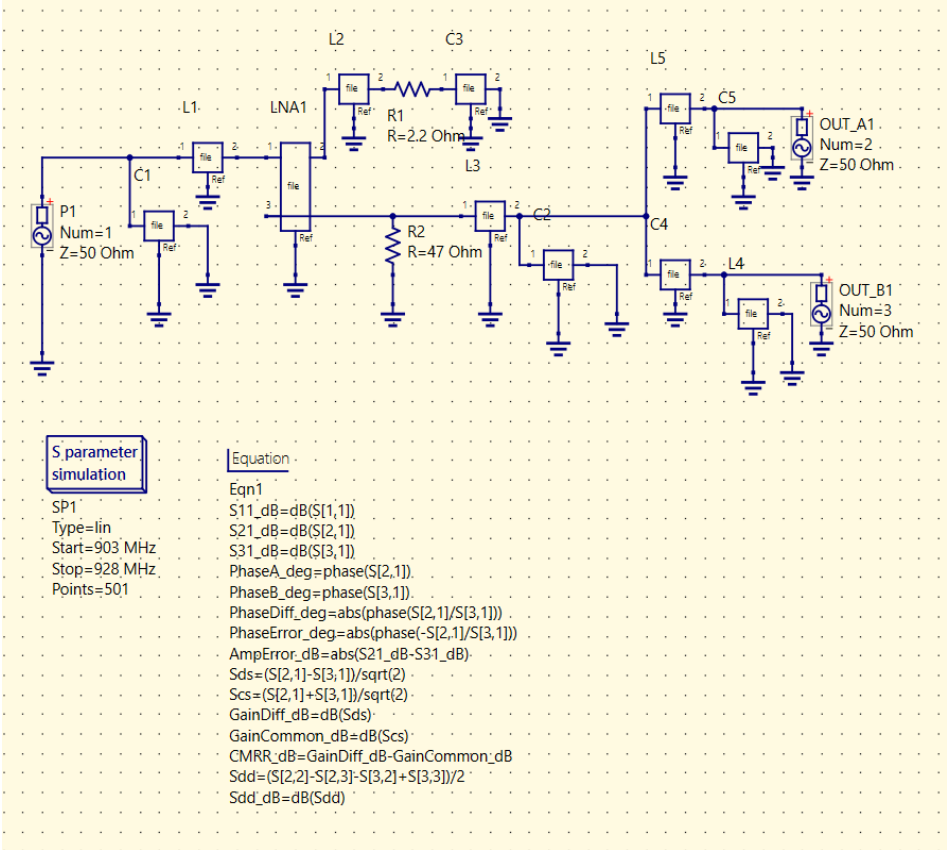


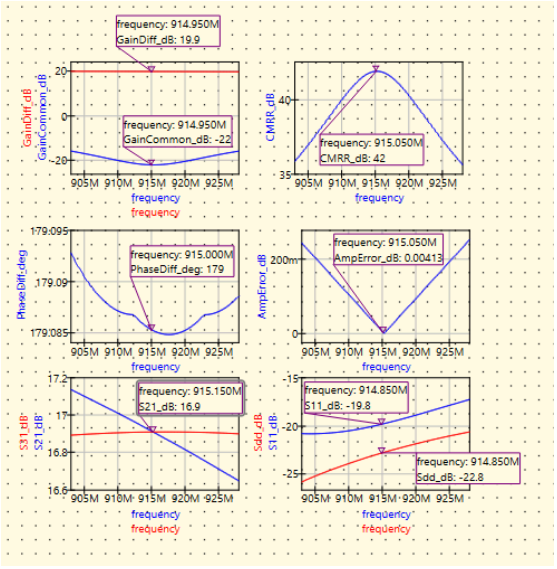


These are the given output results after replacing everything with vendor models. The gain and stability are still very consistent. The power delivery changed slightly, but both are still well within a valid range and with only about 1% of power being reflected for the inputs and outputs.

LNA BALUN CONNECTION:

Now that we have designed and simulated a balun and LNA and verified they worked, we can connect the output of the LNA to the input of the balun





Everything still looks good with them connected so the next step is adding a band pass filter before the LNA to filter out the specific range that we want

Band Pass Filter:
The specific one I am choosing is a standard RF filter: the capacitively coupled resonator filter
An ideal parallel LC circuit has its highest impedance at resonance: f0 = 1/(2*pi*sqrt(L*C))
Around resonance it draws very little net current, coupling several of these resonators makes a band-pass response.
I just chose 4.7nH as a starting inductance and solved the capacitance using 915 MHz as the frequency which gave a value of around 6.437 pF for resonator capacitance.

I want to design the filter with around a 100 MHz bandwidth, so FBW = 100/915 = 0.1093
=> Use a butterworth prototype with coefficients g1=1, g2=2, g3=3

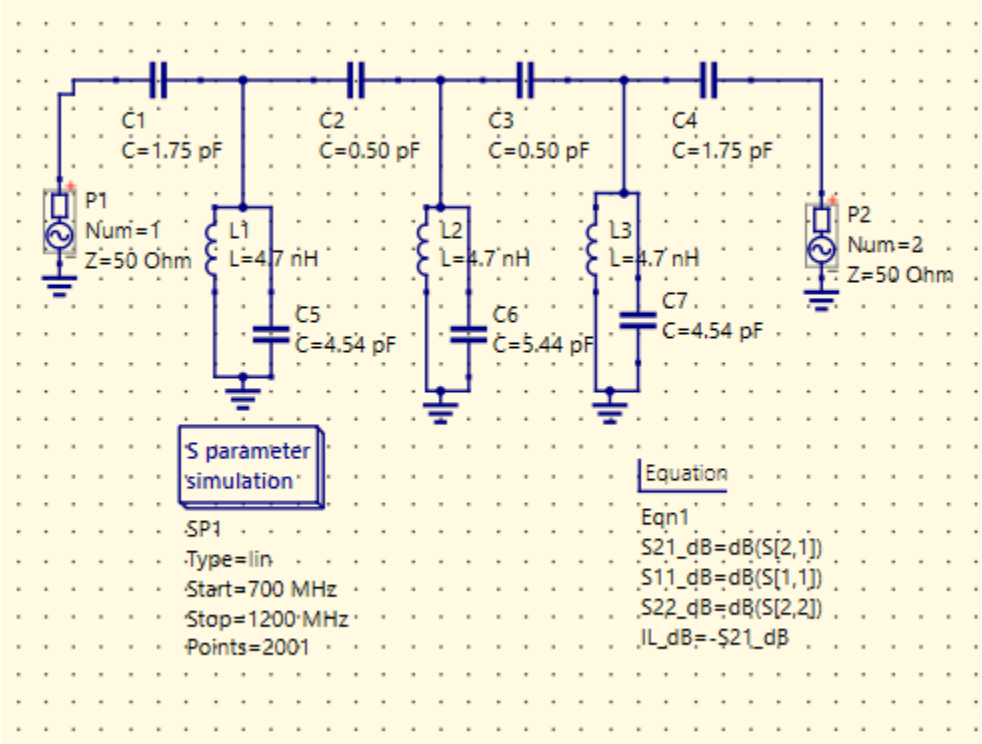
This means to solve for our internal coupled-resonators (The ones between the parallel networks) These are the capacitors that control how strongly the adjacent resonators can exchange energy
C2 = C3 = C0*FBW / sqrt(g1*g2) = 0.497 pF or around **0.50 pF**

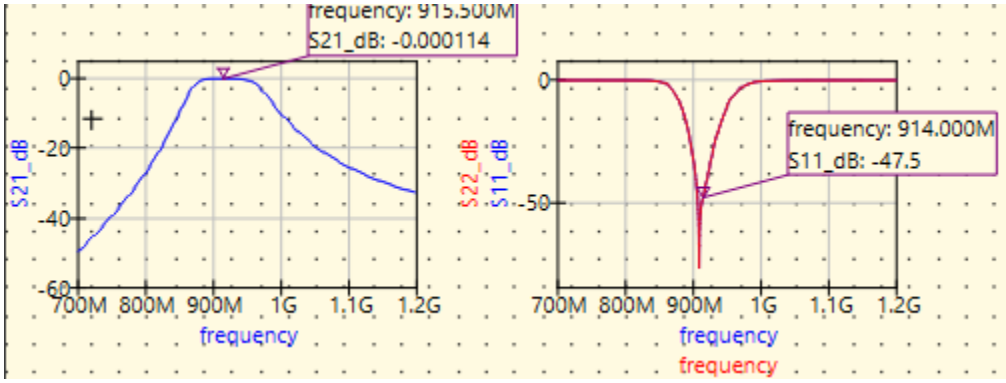
The end capacitors that connect to the source and load require different coupling from the resonator-to resonator connections.
First you calculate the external quality factor, which is how strong the port loads the resonator.
For a butterworth prototype g0g1 = 1, FBW is the same as before and
Qe = (g0g1)/FBW = 9.15
Then for a parallel LC resonator loaded by resistance Rp
Qe = Rp/(w0 * L)
So we solve for resistance, Rp = Qe * w0 * L = 247.24 Ohms
This means we need the capacitor to make the 50 ohm port appear as approximately 247 ohms of parallel resistance at 915 MHz
Looking from the resonator through the capacitor towards the port
Zport = R - jXc
Yport = (R + jXc)/(R^2 + Xc^2)
The real part gives the equivalent parallel resistance
Rp = (R^2 + Xc^2)/R
Solving for Xc = sqrt(Rp*R - R^2) = 99.31 Ohms
Convert that back into capacitance
C0 = 1/(2*pi*f0*Xc) = 1.752*10^-12, so for **C1 and C4** we select values of **1.75 pF**

Now you can calculate the actual capacitors within the RC loops, with the capacitance calculated earlier (C0 = 6.437pF)
The capacitor within the middle loop as capacitors of value 0.50 pF on each side, so
C6 = C0 - C2 - C3 = 5.44pF

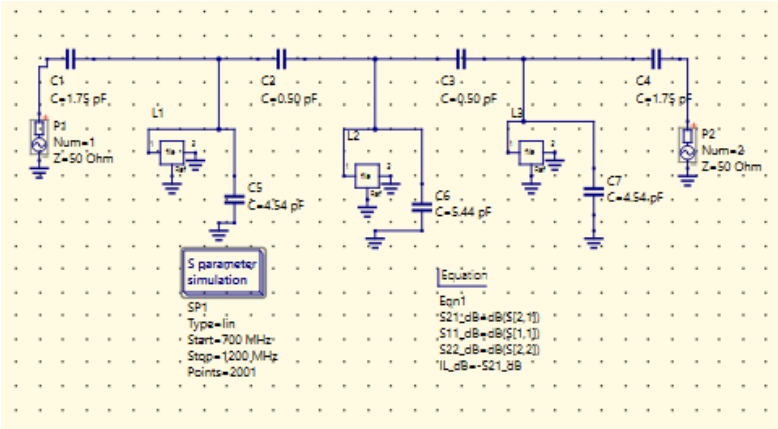
The two end capacitors each have a 0.50 pF and a 1.75 pF capacitor connected to its node. However, the 1.75 pF capacitors connect through resistance. Meaning their actual capacitance contributions are Ceq = Ce/(1 + (w0 * R * Ce)^2) = 1.3966 pF
And so C5 = C7 = C0 - 0.50 - 1.3966 = 4.54 pF

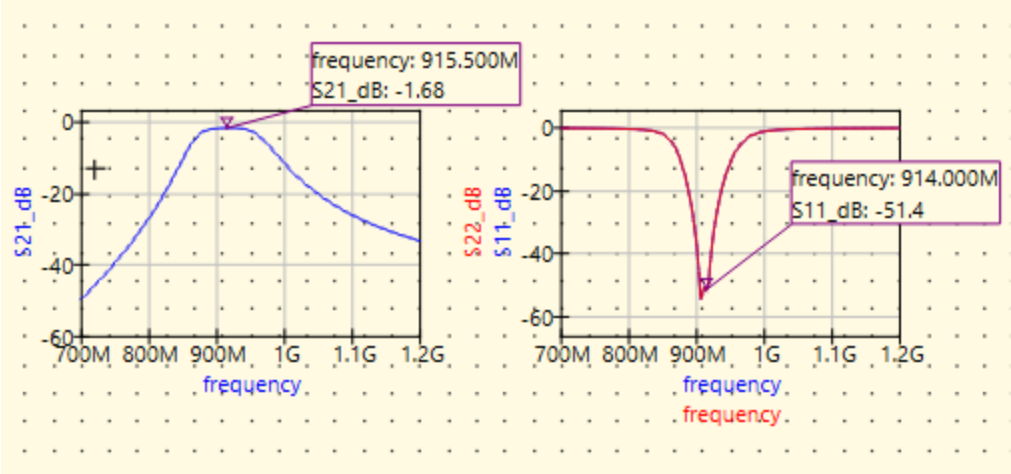
Now with all the capacitor values we can construct the circuit:

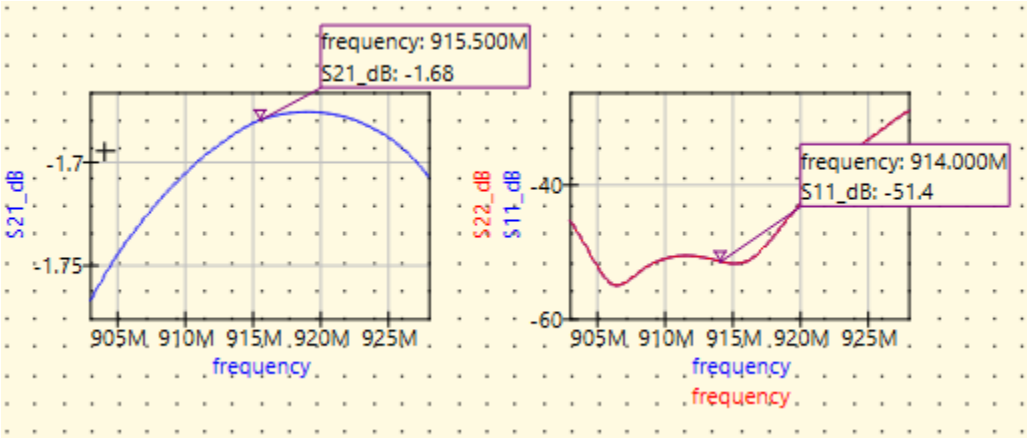




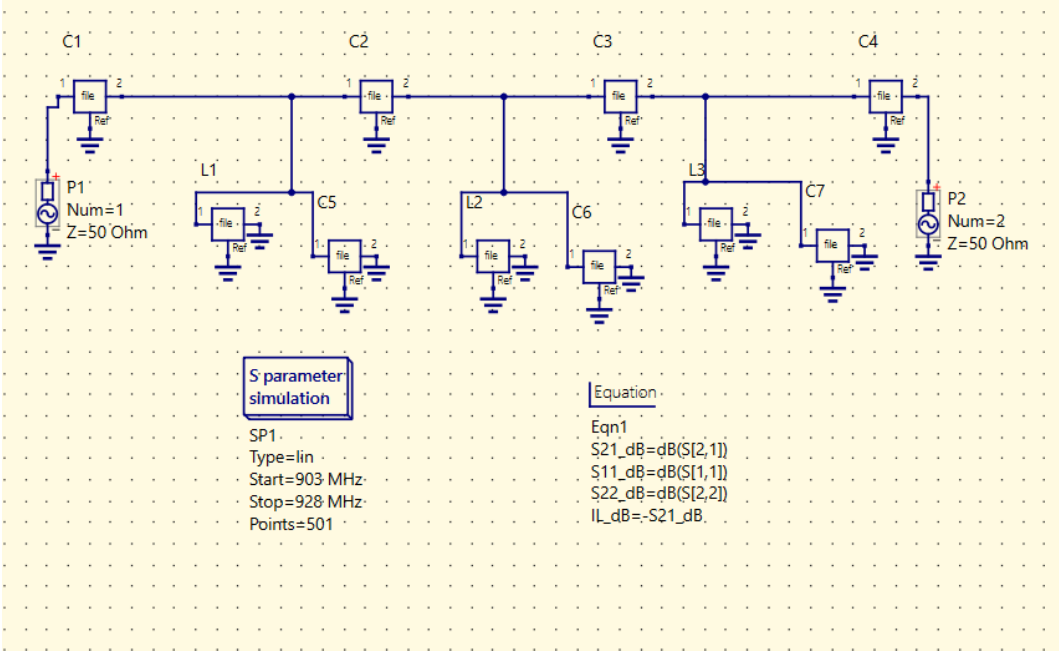
Inductor Vendor Models:

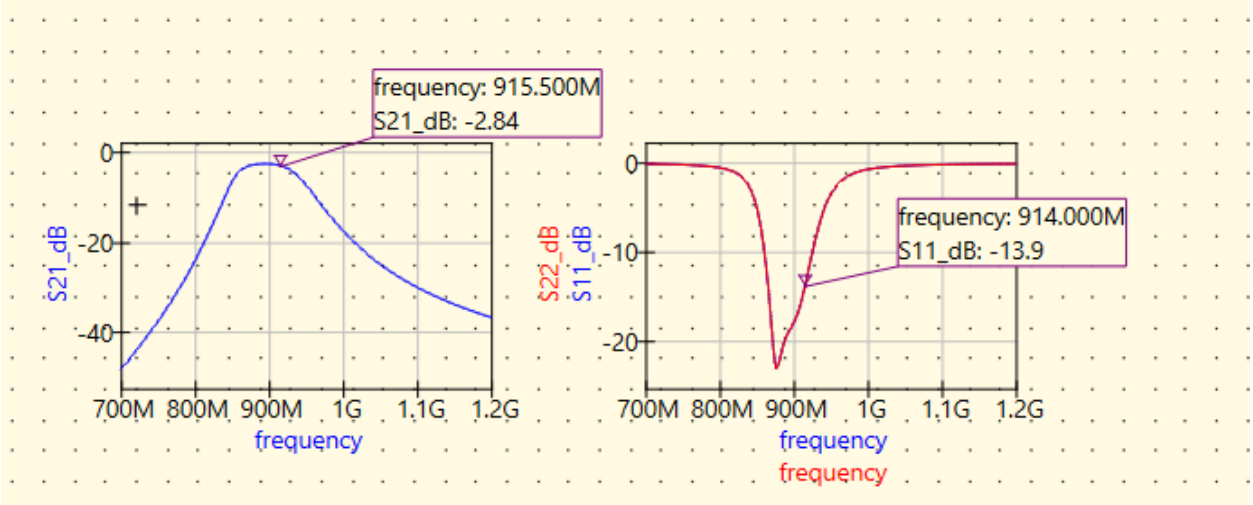






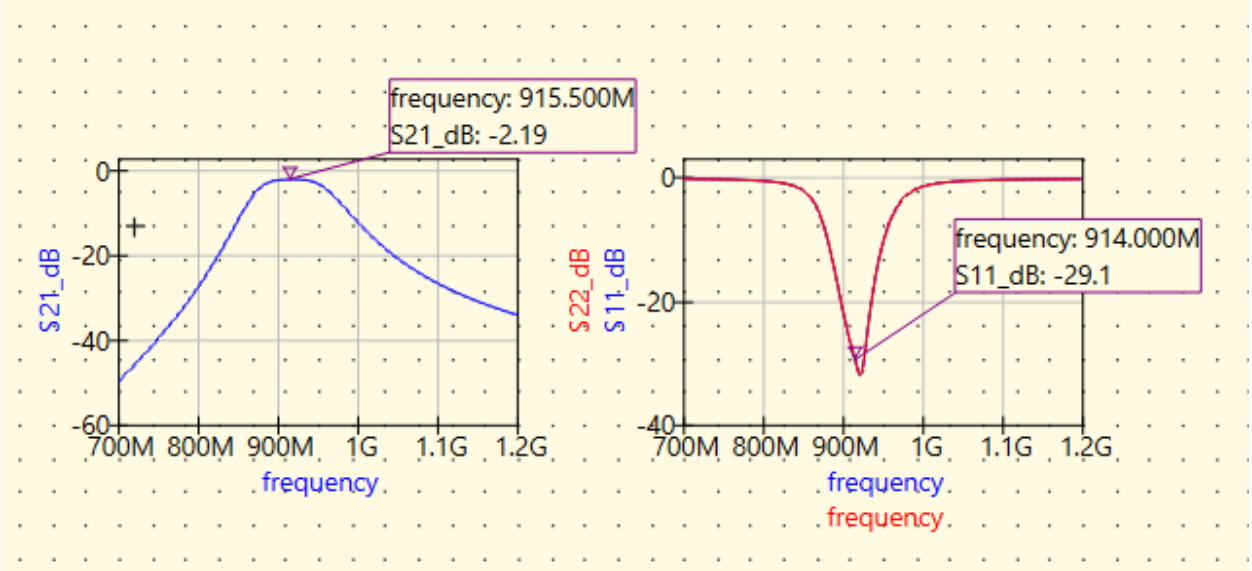
When replacing the capacitors, the **C1, C4: 1.75pF** -> **1.8pF**, **C5, C7: 4.54pF -> 4.5pF**, **C6: 5.44pF -> 5.4 pF,** C5 stayed as 0.50 pF, due to part availability





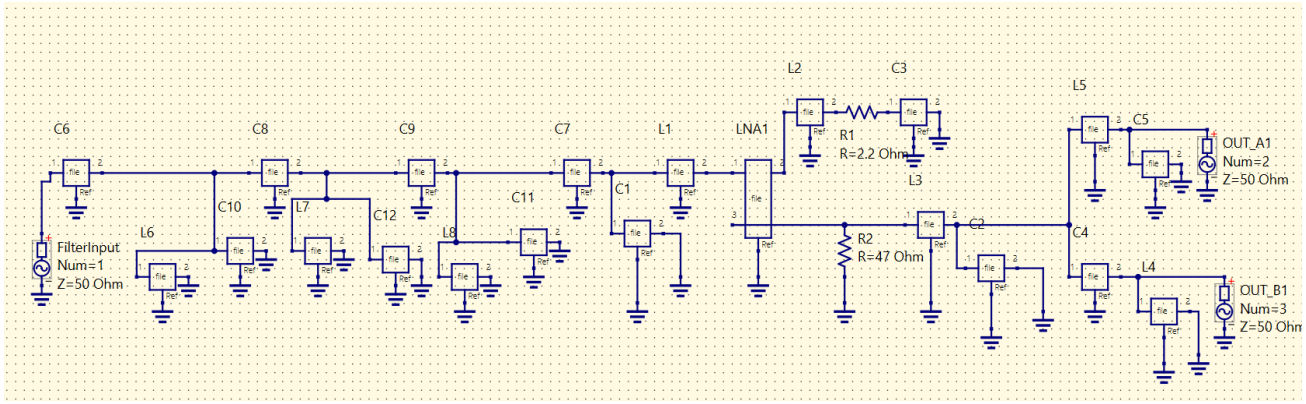
These component models shifted the tuning and increased the loss so I will try to change the capacitor values to adjust. I am adjusting **C5 and C7 from 4.5pF to 4.3pF and C6 from 5.4pF to 5.1pF**

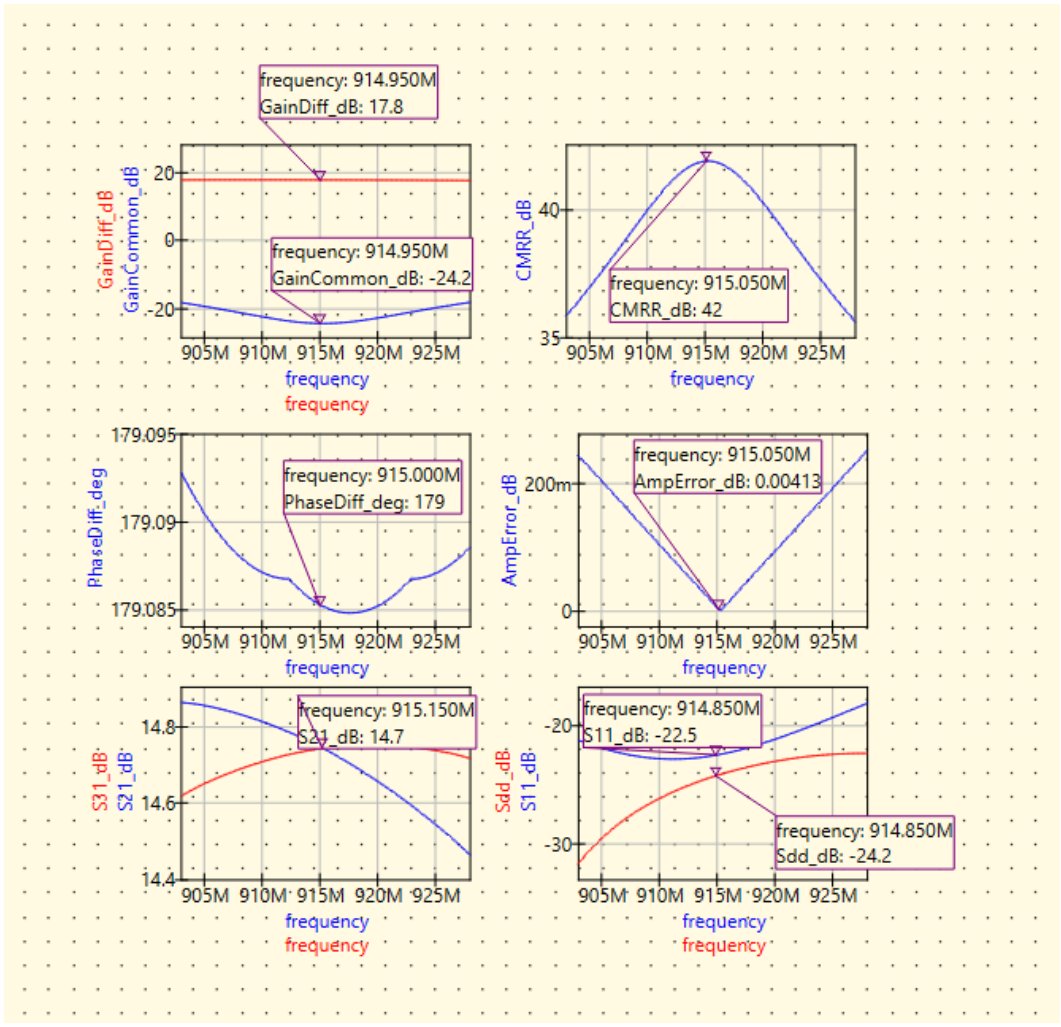
The circuit layout stayed the same, but after adjusting the capacitance values, the filter and power delivered are much more within the desired range.



With this band pass filter being good, we can now attach it to the LNA and balun

Full Circuit:





The top left graph is the differential and common mode gain. You want common mode gain to be as small as possible so you can reduce as much unwanted noise as possible. Differential gain is the main amplification part for your signal

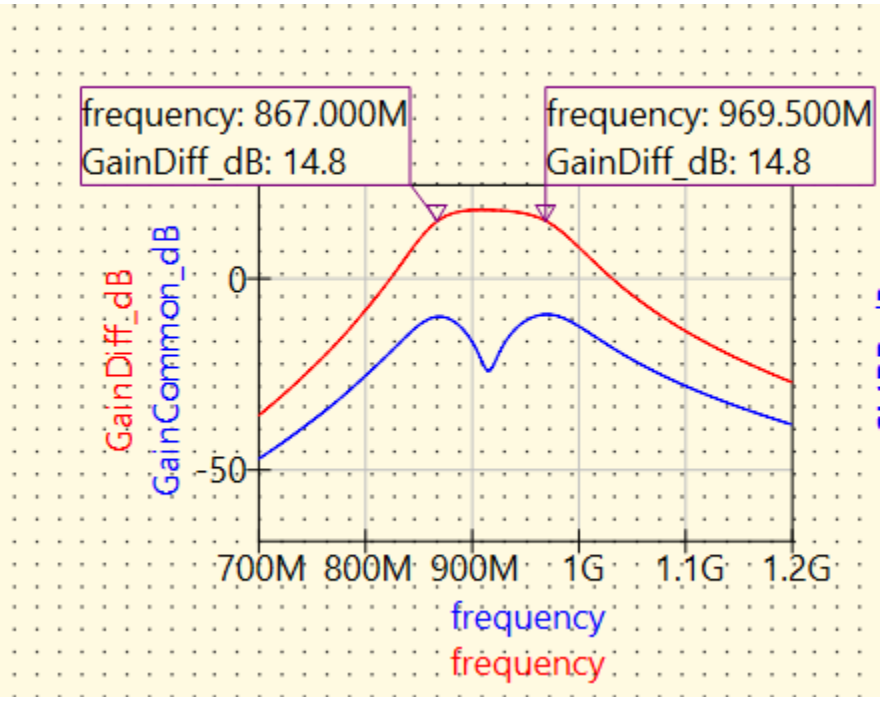
CMRR is the difference between differential and common mode gain, higher CMRR means cleaner differential output.

The middle left graph is phase difference which measures how far apart the two output signals are in phase. The ideal is 180 degrees so that you have two perfectly mirrored signals.

The middle right graph is amplitude error. Zero means equal output amplitudes for your signals. You want a very small output amplitude mismatch.

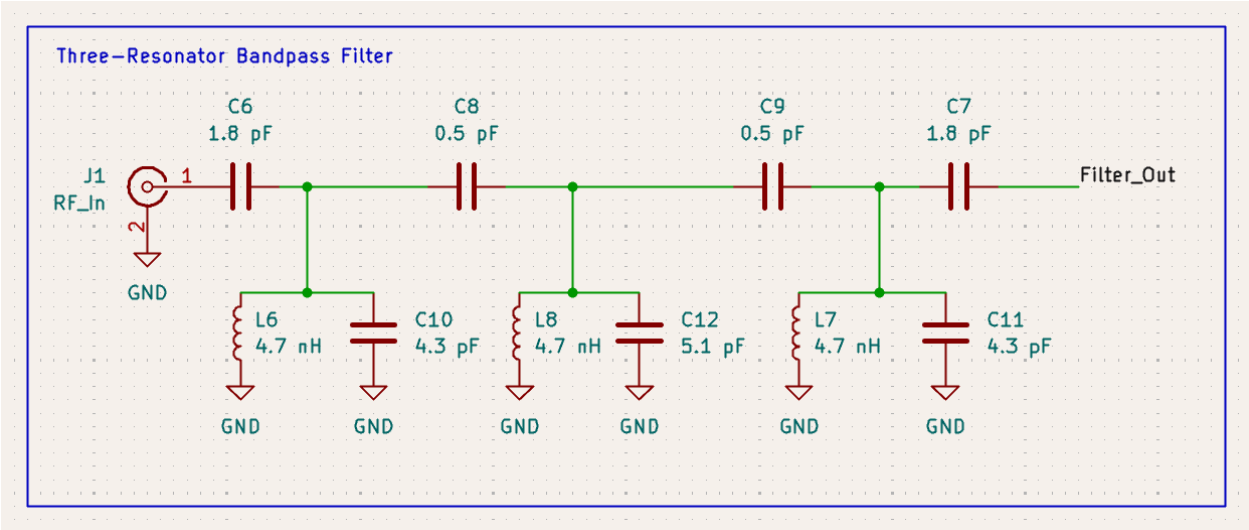
The bottom left graph is the output gains S21 and S31 which show how the signal transfers from the input to each output. The differential gain is around 3dB higher than each branch individually because it combines both outputs so that reference is around 100 ohms.

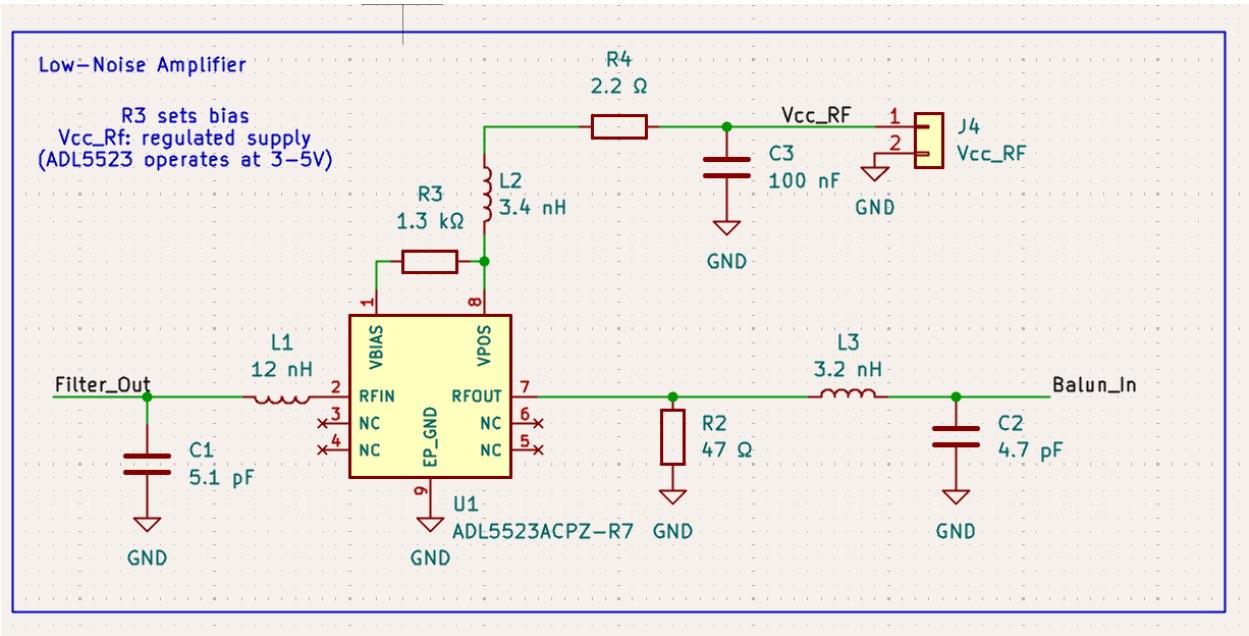
The bottom right graph is the input and differential output matching. The S11_dB checks the input against its 50 ohm reference and around 0.56% of incident power is reflected. Sdd_dB checks the impedance looking into the 100 ohm differential output port, with around 0.38% of power reflected.

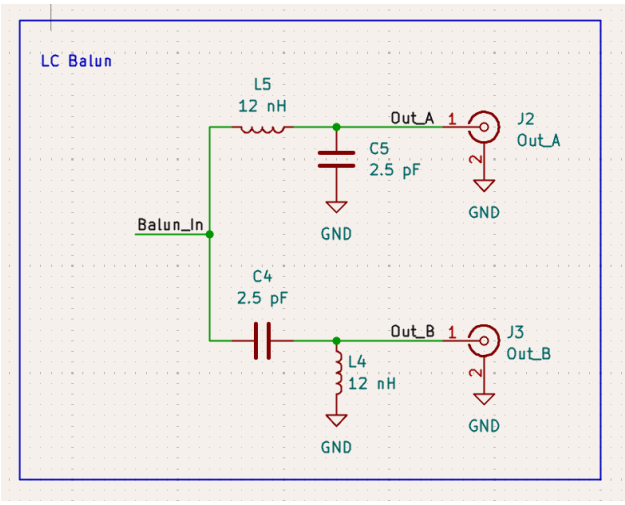


This is a graph of the gain over a wider frequency and where the Differential reaches -3dB from the peak. So we can calculate our bandwidth from 969.5 - 867 = 102.5MHz which is over our 100Mhz design target.

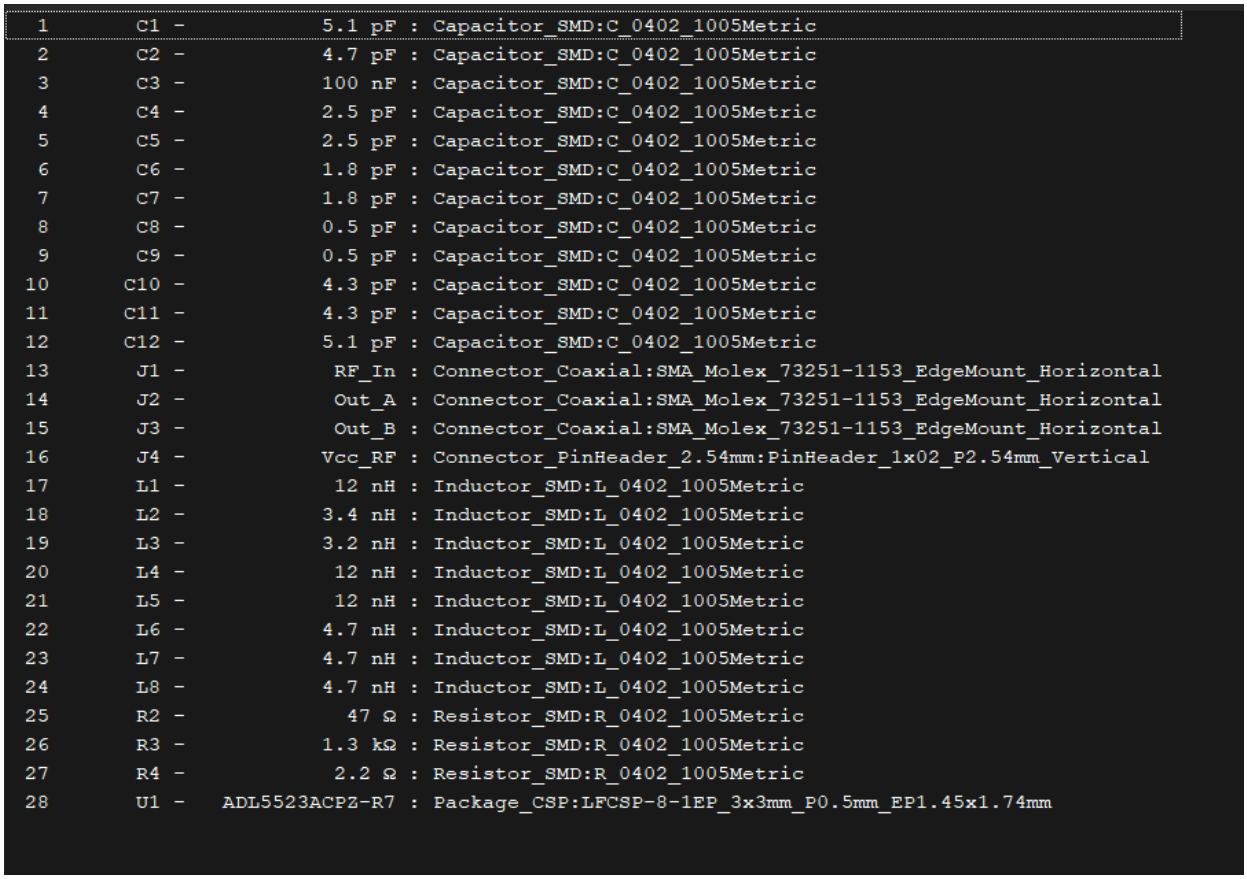
Now we have the full circuit, we can build it in KiCad


Three-Resonator Bandpass Filter
C6
1.8 pF
C8
0.5 pF
C9
0.5 pF
C7
1.8 pF
J1
RF_In
1
2
GND
Filter_Out
L6
4.7 nH
C10
4.3 pF
L8
4.7 nH
C12
5.1 pF
L7
4.7 nH
C11
4.3 pF
GND


Low-Noise Amplifier
R3 sets bias
Vcc_Rf: regulated supply
(ADL5523 operates at 3-5V)
R4
2.2 Ω
Vcc_RF
J4
Vcc_RF
C3
100 nF
R3
1.3 kΩ
L2
3.4 nH
L1
12 nH
Filter_Out
VBIAS
VPOS
RFIN
RFOUT
NC
NC
NC
NC
EP_GND
L3
3.2 nH
Balun_In
C1
5.1 pF
R2
47 Ω
C2
4.7 pF
U1
ADL5523ACPZ-R7
GND


LC Balun
L5
12 nH
Out_A
J2
Out_A
C5
2.5 pF
Balun_In
C4
2.5 pF
Out_B
J3
Out_B
L4
12 nH
GND

Now we can assign footprints:



1	C1 -	5.1 pF	: Capacitor_SMD:C_0402_1005Metric
2	C2 -	4.7 pF	: Capacitor_SMD:C_0402_1005Metric
3	C3 -	100 nF	: Capacitor_SMD:C_0402_1005Metric
4	C4 -	2.5 pF	: Capacitor_SMD:C_0402_1005Metric
5	C5 -	2.5 pF	: Capacitor_SMD:C_0402_1005Metric
6	C6 -	1.8 pF	: Capacitor_SMD:C_0402_1005Metric
7	C7 -	1.8 pF	: Capacitor_SMD:C_0402_1005Metric
8	C8 -	0.5 pF	: Capacitor_SMD:C_0402_1005Metric
9	C9 -	0.5 pF	: Capacitor_SMD:C_0402_1005Metric
10	C10 -	4.3 pF	: Capacitor_SMD:C_0402_1005Metric
11	C11 -	4.3 pF	: Capacitor_SMD:C_0402_1005Metric
12	C12 -	5.1 pF	: Capacitor_SMD:C_0402_1005Metric
13	J1 -	RF_In	: Connector_Coaxial:SMA_Molex_73251-1153_EdgeMount_Horizontal
14	J2 -	Out_A	: Connector_Coaxial:SMA_Molex_73251-1153_EdgeMount_Horizontal
15	J3 -	Out_B	: Connector_Coaxial:SMA_Molex_73251-1153_EdgeMount_Horizontal
16	J4 -	Vcc_RF	: Connector_PinHeader_2.54mm:PinHeader_1x02_P2.54mm_Vertical
17	L1 -	12 nH	: Inductor_SMD:L_0402_1005Metric
18	L2 -	3.4 nH	: Inductor_SMD:L_0402_1005Metric
19	L3 -	3.2 nH	: Inductor_SMD:L_0402_1005Metric
20	L4 -	12 nH	: Inductor_SMD:L_0402_1005Metric
21	L5 -	12 nH	: Inductor_SMD:L_0402_1005Metric
22	L6 -	4.7 nH	: Inductor_SMD:L_0402_1005Metric
23	L7 -	4.7 nH	: Inductor_SMD:L_0402_1005Metric
24	L8 -	4.7 nH	: Inductor_SMD:L_0402_1005Metric
25	R2 -	47 Ω	: Resistor_SMD:R_0402_1005Metric
26	R3 -	1.3 kΩ	: Resistor_SMD:R_0402_1005Metric
27	R4 -	2.2 Ω	: Resistor_SMD:R_0402_1005Metric
28	U1 -	ADL5523ACPZ-R7	: Package_CSP:LFCSP-8-1EP_3x3mm_P0.5mm_EP1.45x1.74mm

For the capacitors, the Murata capacitors in my simulations used 0402 imperial / 1005 metric packages (0.04 inches W * 0.02 inches L) / (1.0mm * 0.5mm)
For the inductors, the coilcraft 0402DC all share the standard inductor footprint shown in the screenshot
For R2, R3, R4, I selected 0402 chip resistors to keep the RF connections compact.
For connectors J1-J3, the footprint specifically is the **Molex 73251-1153 SMA connector**, which is specified for a 1.6mm PCB and 50 Ohm impedance
For J4, I chose a standard two-pin 2.54 mm pitch, through hole header for connecting external power
For the Low-noise Amplifier U1, the ADL5523 uses a CP-8-13 package which is a 3x3mm body, 0.5 mm lead pitch, eight leads, and an exposed ground pad.

The main walkthrough for selection is:

- Identify actual manufacturer part number from simulation
- Read its package drawing and recommended PCB land pattern
- Find matching KiCad footprint
- Check that every pad number corresponds to correct schematic pin

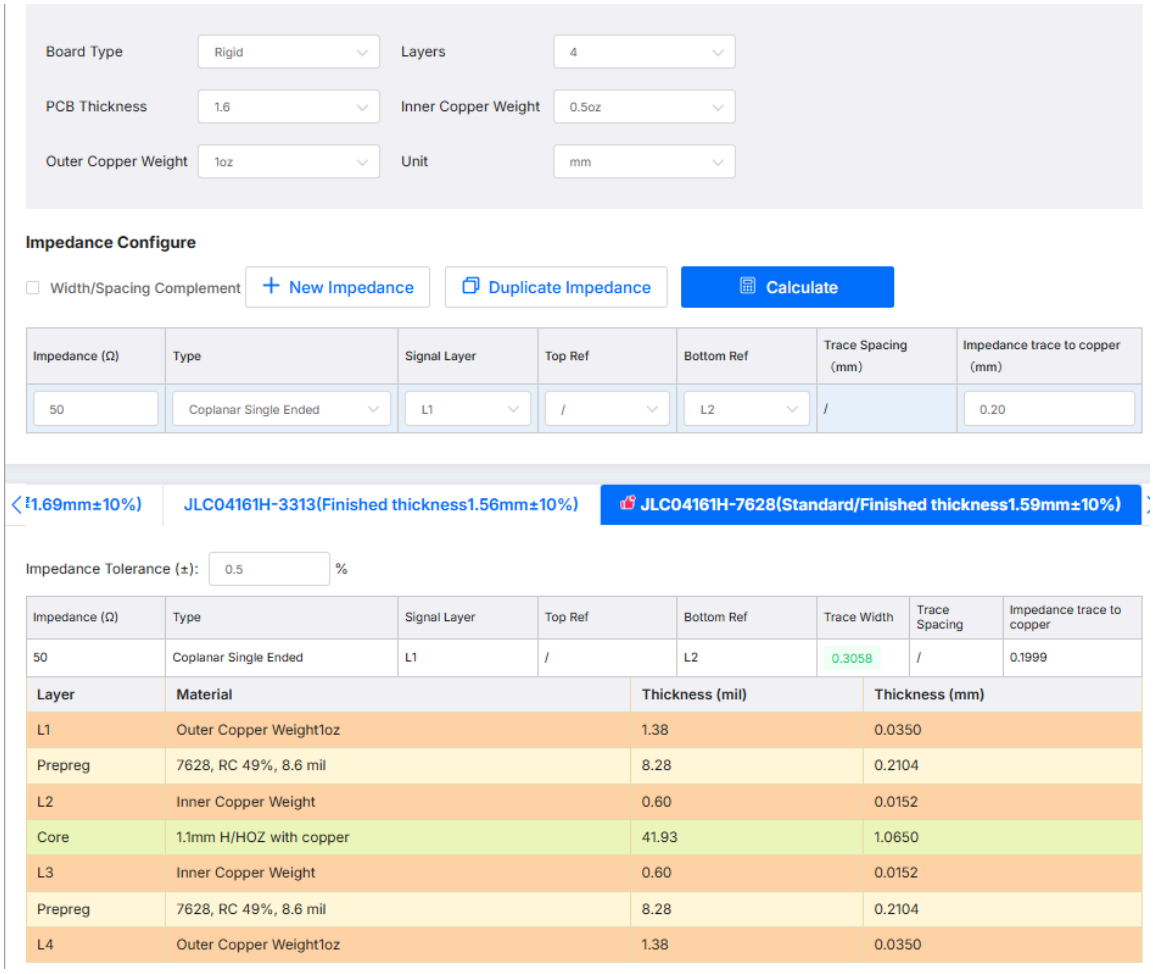
Run ERC again after adding footprints
After it verifies there are no violations, we can move on to actual PCB Layout

Before starting, I want to define the four layer stackup. I used JLPCB'S JLC0415H-7628, 1.6mm construction as the reference
https://jlcpcb.com/impedance
A four-layer setup is better for an RF circuit because you can put a continuous ground plane closer to the RF signals. Being able to place the main RF ground reference only 0.2104mm under the signal layer gives it a very short return current loop.
The planned layer use is:

- F.Cu: RF components and traces
- In1.Cu: Main RF ground reference
- In2.Cu: Ground reference for bottom-layer routing
- B.Cu: DC power routing and ground copper

The inner layers are chosen as ground references so they can remain uninterrupted. Having them next to each other also allows them to more easily connect to the same ground net with vias

The next thing to decide is the trace geometry. I will use a grounded coplanar waveguide: A top-layer RF trace with ground copper beside it and the inner ground plane underneath.
I used the JLCPCB calculator and it returned a 0.3058mm width with a 0.20 gap to adjacent ground copper.



Board Type	Rigid	Layers	4
PCB Thickness	1.6	Inner Copper Weight	0.5oz
Outer Copper Weight	1oz	Unit	mm

Impedance Configure

Width/Spacing Complement | + New Impedance | Duplicate Impedance | Calculate

Impedance (Ω)	Type	Signal Layer	Top Ref	Bottom Ref	Trace Spacing (mm)	Impedance trace to copper (mm)
50	Coplanar Single Ended	L1	/	L2	/	0.20

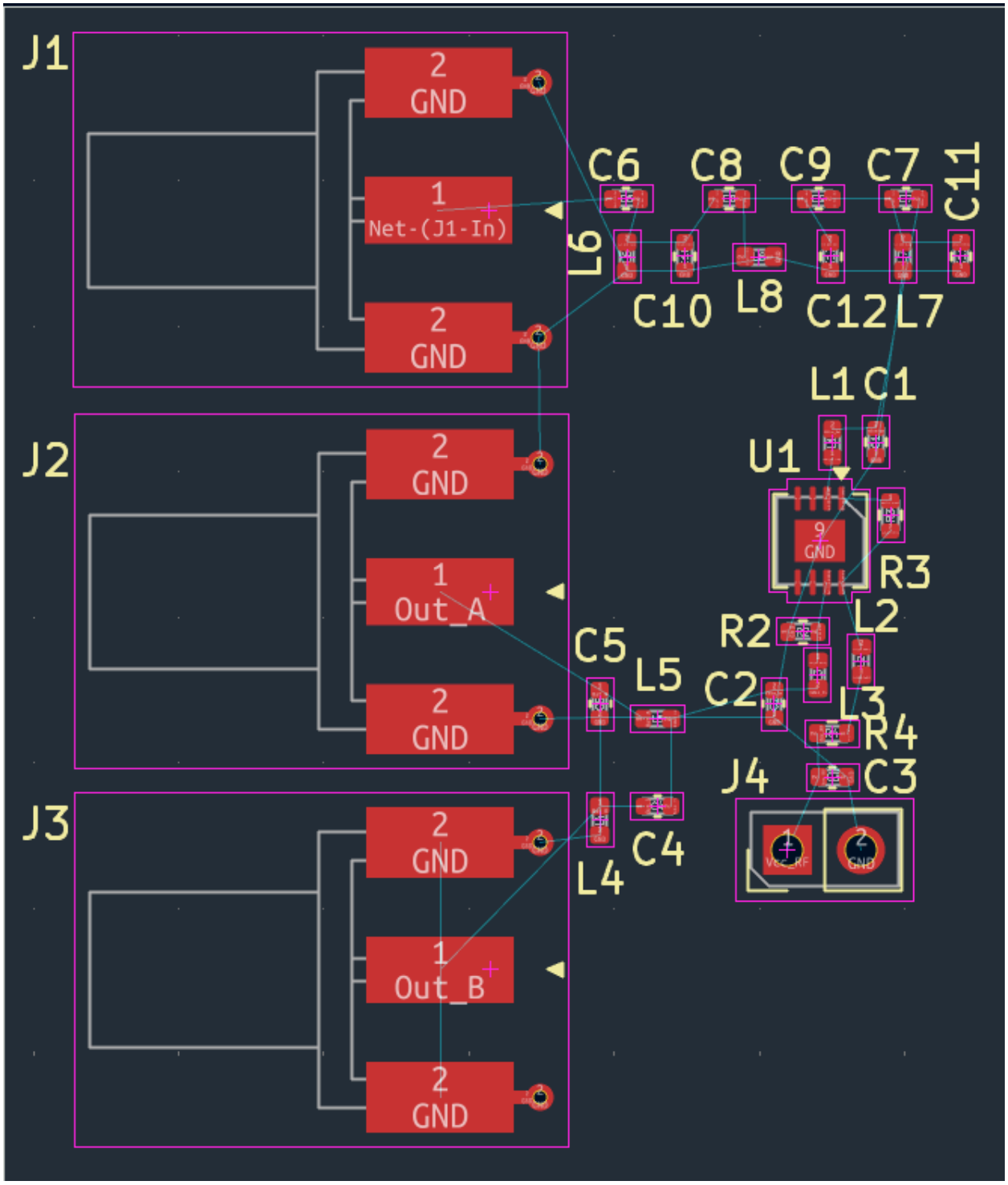
1.69mm±10%) | JLC04161H-3313(Finished thickness1.56mm±10%) | JLC04161H-7628(Standard/Finished thickness1.59mm±10%)

Impedance Tolerance (±): 0.5 %

Impedance (Ω)	Type	Signal Layer	Top Ref	Bottom Ref	Trace Width	Trace Spacing	Impedance trace to copper
50	Coplanar Single Ended	L1	/	L2	0.3058	/	0.1999

Layer	Material	Thickness (mil)	Thickness (mm)
L1	Outer Copper Weight1oz	1.38	0.0350
Prepreg	7628, RC 49%, 8.6 mil	8.28	0.2104
L2	Inner Copper Weight	0.60	0.0152
Core	1.1mm H/HOZ with copper	41.93	1.0650
L3	Inner Copper Weight	0.60	0.0152
Prepreg	7628, RC 49%, 8.6 mil	8.28	0.2104
L4	Outer Copper Weight1oz	1.38	0.0350

Then we can place the components



In this layout I opted to have all the connectors on the left just for consistency.

C6 is placed immediately to the right of the input so there is a direct path for the RF signal. The entire filter sits relatively compact to keep the signal as clean as possible. Inductor L8 (in the middle resonator) was rotated to reduce possible magnetic coupling between the resonators.

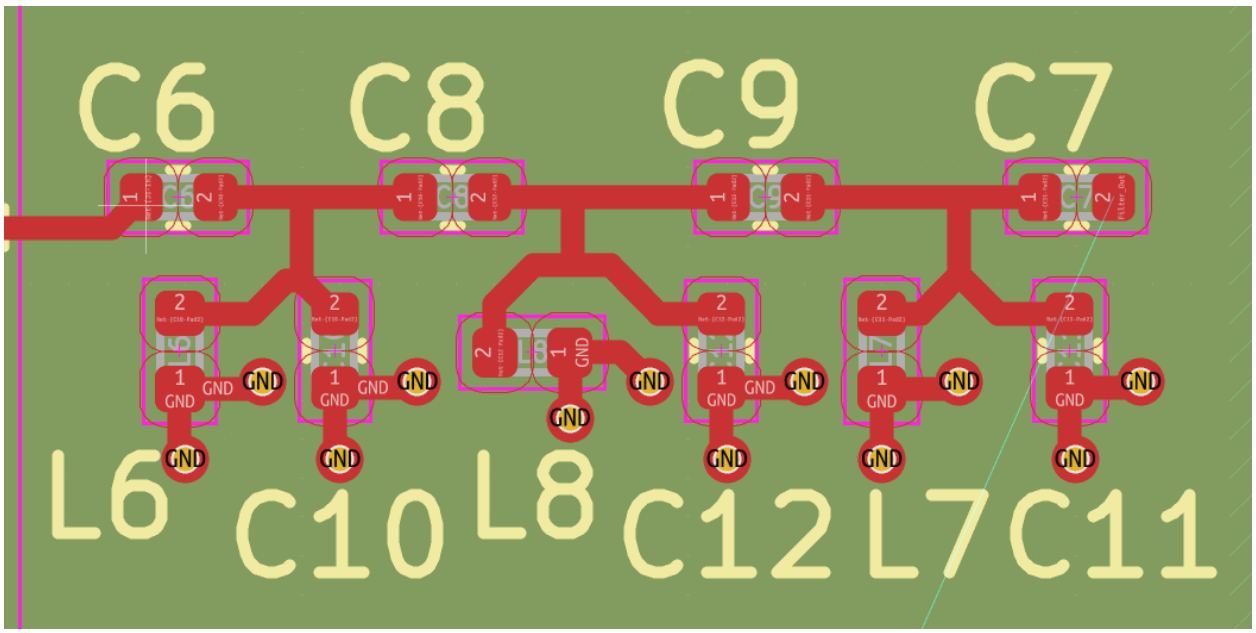
The output of the filter, C7, then leads into C1 and L1. These are the two components that form the input matching network. These are placed as close to the input of the LNA as possible because long connections might change the impedance presented to the amplifier.

L3 and C2 form the output matching network and are also kept close to the output of the LNA to make sure the output impedance is as close to the simulation as possible.

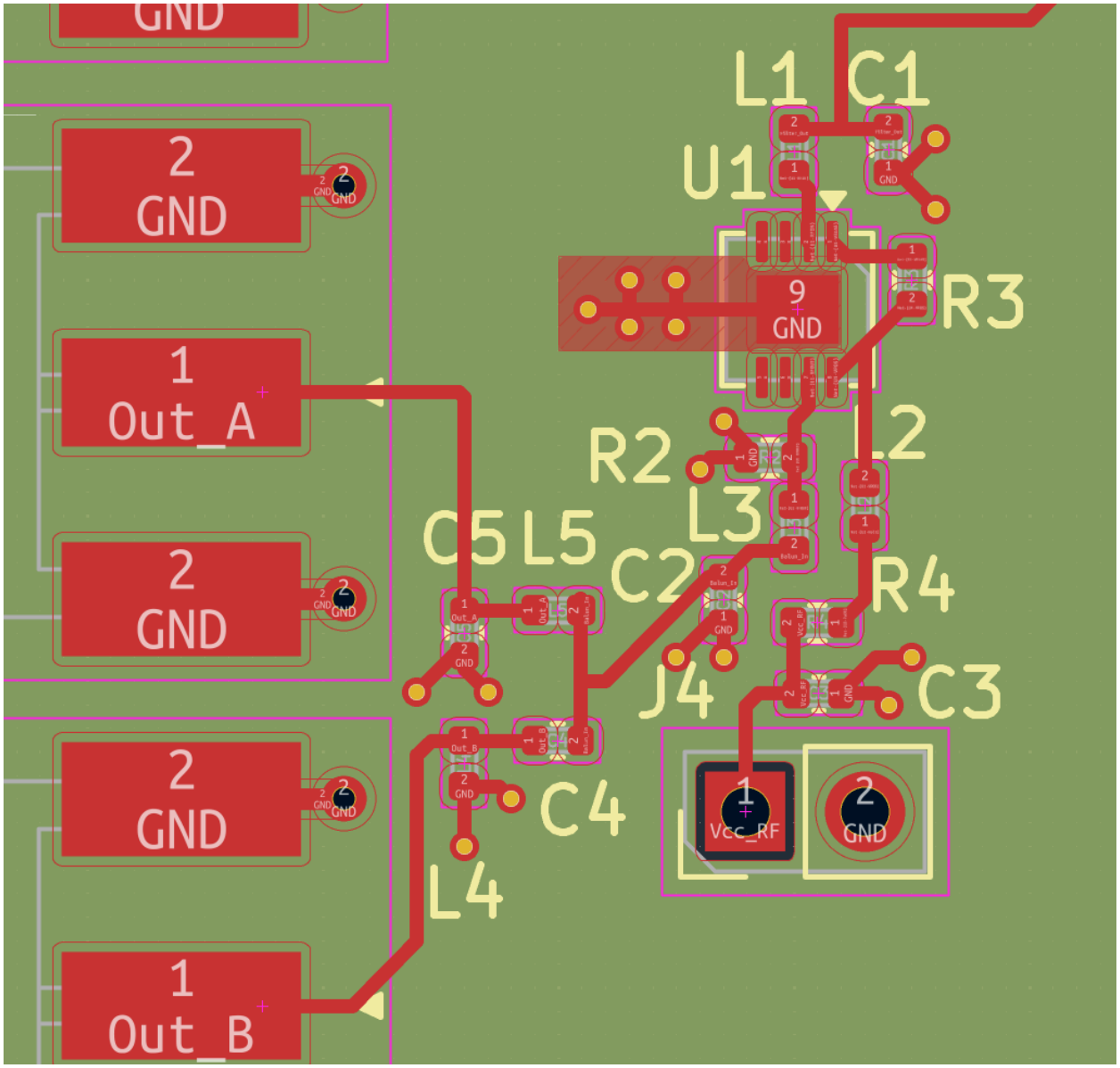
R3 sets the amplifier's bias current. Its connection between pins 1 and 8 make it compact.

R4 and C3 add series supply damping. Keeping these connections close to the reference supply J4 reduces unwanted connection inductance.

For the balun, each branch has an intended phase response that mirrors the other. This means you want similar trace connections and grounding to preserve that 180 degree output difference.



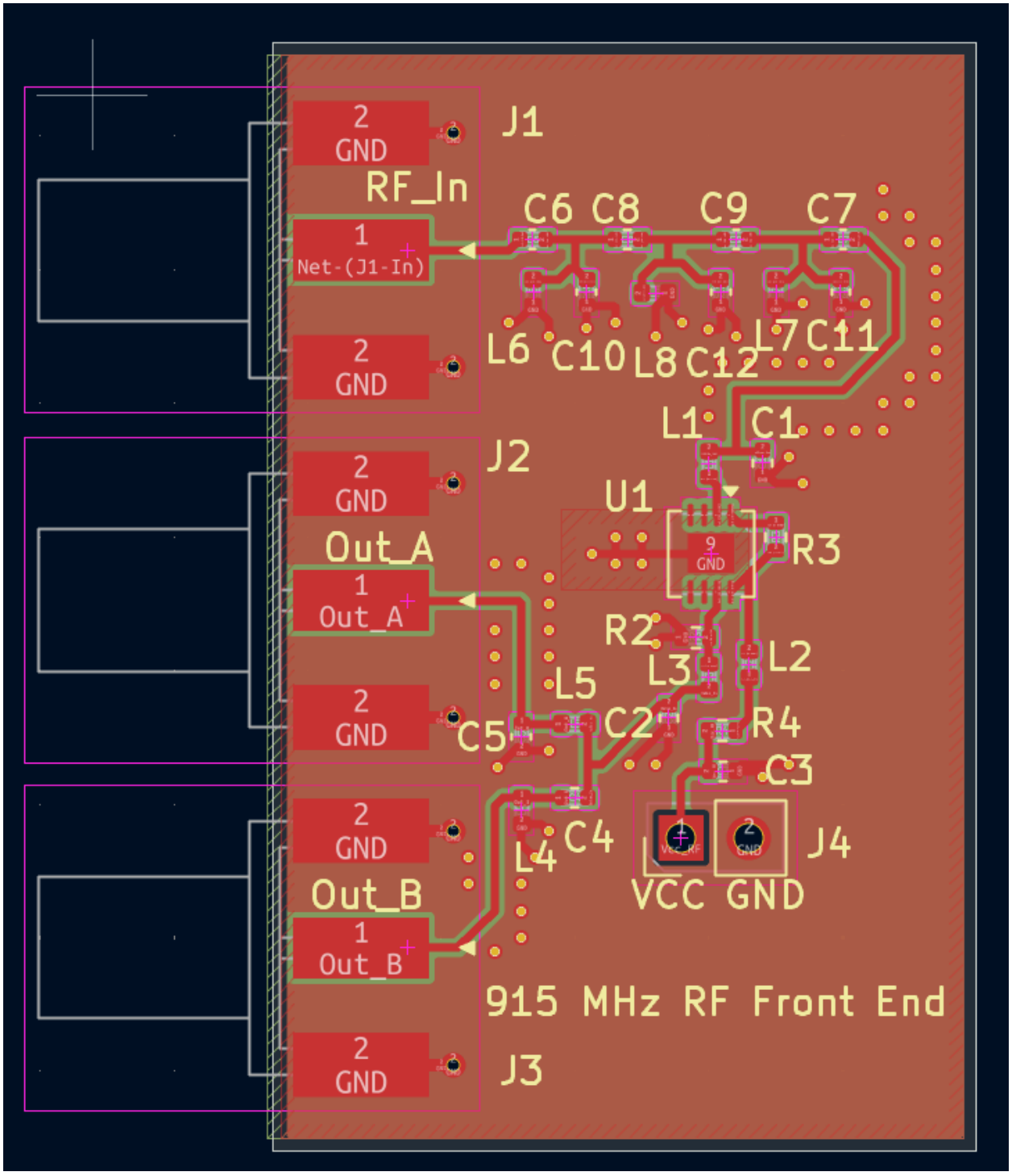
Here I used a two-via ground arrangement with each having short connections to their component's ground pad. Adding a second via improves the RF ground return. Vias have parasitic inductance as well which can add impedance at high frequencies. Adding two nearby vias in parallel generally helps reduce that impedance.

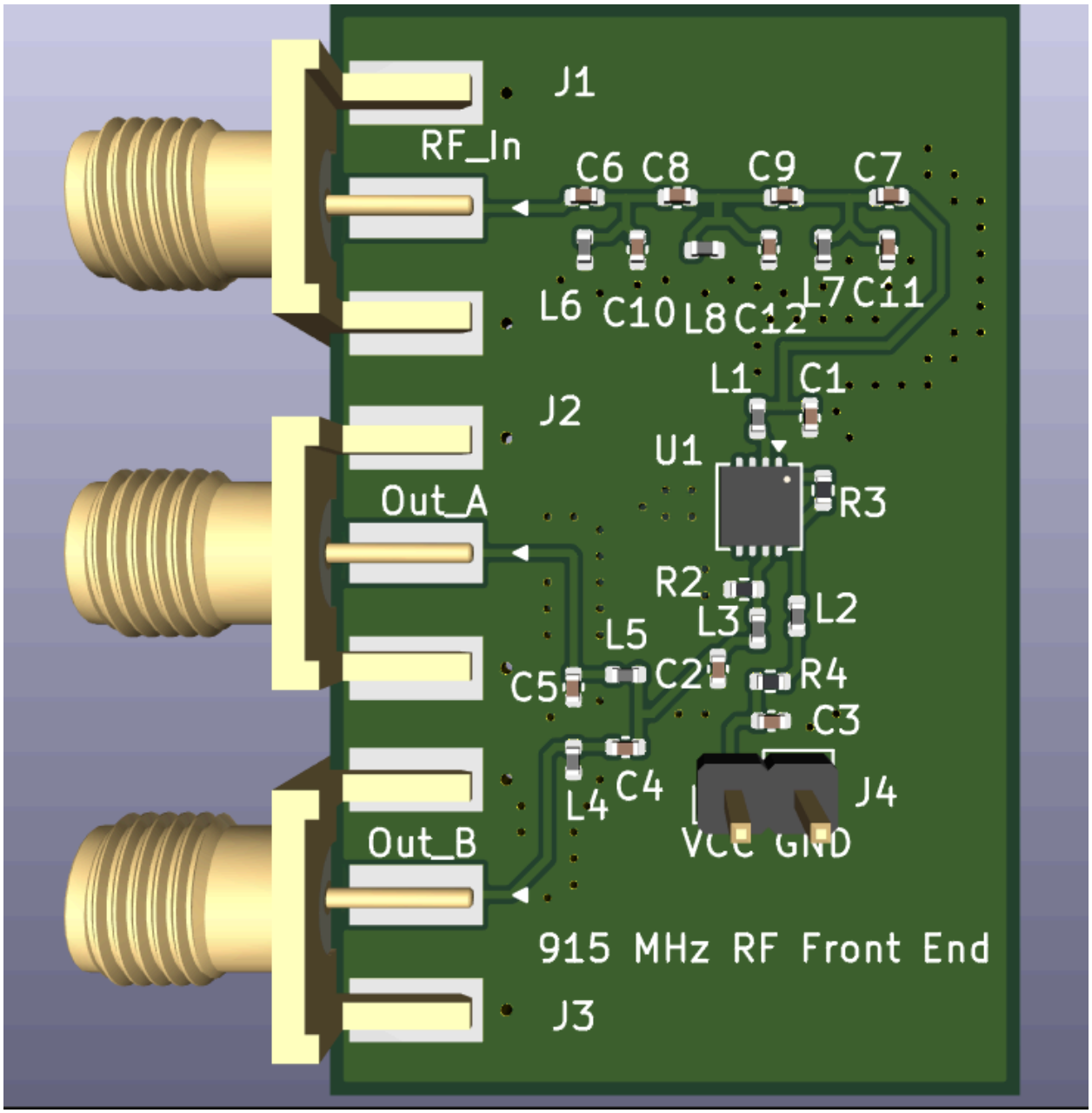


The top of the Filter_Out Connection comes from the output of C7. The outputs of the balun connect to their respective output pad ports. A small ground pad over the five vias connected to the low noise amplifier are included for better return current as well.

One of the more important measurements are the trace lengths of Out_A and Out_B. I made sure I could get them as close as possible. They had lengths of 10.6344 and 10.4597 which is around a 0.1747mm difference. At 915 Mhz that attributes around 0.33 degrees of phase mismatch assuming a dielectric constant of 3.

After doing all of this, I added a ground copper pour over the top of everything again to shield the RF circuit from external noise. Within this ground copper pour, I added stitching vias along the sensitive RF links (Filter output, Out_A, and Out_B)


J1
2
GND
RF_In
1
Net-(J1-In)
2
GND
J2
2
GND
Out_A
1
Out_A
2
GND
J3
2
GND
Out_B
1
Out_B
2
GND
C6
C8
C9
C7
L6
C10
L8
C12
L7
C11
L1
C1
U1
9
GND
R3
R2
L3
L2
L5
C5
C2
R4
C3
C4
L4
J4
VCC
GND
915 MHz RF Front End



The intended connections are an antenna suitable for 915 Mhz at Rf_In and then ADC differential inputs at In+ or In- or a downconversion stage. This board is compatible with a differential ADC that takes In+ and In- inputs.